Remarks

Claims 1-6 are pending in this action. Claims 1 and 3 are objected to, and Claims 1-6 stand rejected. By this amendment claims 1, 3, and 4 have been amended. Applicants respectfully request reconsideration of all pending claims herein.

Applicants respectfully submit that the amendments to claims 1, 3 and 4 more clearly define and claim Applicants' invention and distinguish it over the prior art of record. No new matter has been added to the application by virtue of the present amendment.

Claim Objections

Applicants have amended claims 1 and 3. In claim 1, Applicants have amended the claim to include the claim number "1". Applicants have amended claim 3, last line to state "…in order synchronously…", as is observed in parallel method claim 6. Applicants submit that the objection to claims 1 and 3 described in the Office Action has been overcome.

Claim Rejections – 35 U.S.C. §112, Second paragraph

The Office Action stated that claims 1-3 stand rejected under 35 U.S.C. §112, second paragraph, as failing to include one or more claims at the conclusion of the specification which particularly point out and distinctly claim the subject matter which the applicant regards as his invention. Specifically, the Office Action stated that claim 1 is an apparatus claim, yet has language pertaining to a method claim.

Applicants have amended claim 1 to be in compliance with MPEP 2173.05(p). Claim 1 now reads, in part, "~~activating~~ said sense amplifiers adapted to activate when enabled by a ~~using an~~ sense amplifier enable signal;"

Applicants have amended claim 1, to clarify the claimed invention, as noted above. Accordingly, Applicants respectfully submit that the rejection of claims 2 – 3 under 35 U.S.C. §112 second paragraph have been overcome by virtue of their dependence on amended claim 1.

Claim Rejections - 35 U.S.C. § 102(b)

The Office Action stated that claims 1-6 stand rejected under 35 USC §102(b) as being anticipated by Fujisawa et al. (U.S. Patent Publication No. 2004/0004890). Specifically, regarding claims 1 and 4 the Office Action stated that Fujisawa et al. discloses a semiconductor memory and its corresponding burst operation method for the semiconductor memory.

Applicants submit that Fujisawa does not teach or disclose Applicants latches as described in claim 1: "A semiconductor memory, comprising: data I/O buses; a plurality of *latch circuits* connected in common to each of said data I/O buses…" (see Applicants figs. 2 and 3 PFPLL, and pg. 11-12 paragraphs 0055-57). The Office Action stated that Fujisawa discloses buffer circuits and stated that the buffer circuits were the same as Applicant's latches (see Office Action pg. 3 item 7). However, Applicant's latches PFPLL are separate elements and are coupled between buffer circuits (WB) and the secondary sense amplifiers, and the I/O buses (see Applicant's figures 2 and 3 and paragraphs 55-57). The output circuit of Fujisawa shows/describes buffers connected directly to I/O lines, which are further connected to the main sense amplifiers and not sub amplifiers (Fujisawa Fig. 1 output circuit 18, paragraphs 0046-0047). Therefore, Fujisawa does not anticipate Applicant's claim 1. For the reasons stated above, the latch circuits recited in claim 4 are also not anticipated by Fujisawa. Therefore claims 1 and 4 should pass to issuance.

Accordingly, Applicants respectfully submit that the rejection of claims 1 and 4 under 35 U.S.C. § 102(b) has been overcome. Since Claims 2-3 depend from Claim 1 and Claims 5-6

depend from Claim 4, all claims are in condition for allowance.

Conclusion

Please do not hesitate to call/email the undersigned at the number/email address listed below if there are further questions.

Respectfully submitted,
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